1. Record Nr. UNINA9910139930203321

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Titolo	Transient-induced latchup in CMOS integrated circuits / / Ming-Dou Ker and Sheng-Fu Hsu
Pubbl/distr/stampa	Singapore ; , : Wiley, , c2009 [Piscataqay, New Jersey] : , : IEEE Xplore, , [2010]
ISBN	1-282-38218-7 9786612382185 0-470-82409-3 0-470-82408-5
Descrizione fisica	1 online resource (265 p.)
Altri autori (Persone)	HsuSheng-Fu
Disciplina	621.3815 621.39/5
Soggetti	Metal oxide semiconductors, Complementary - Defects Metal oxide semiconductors, Complementary - Reliability
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Physical Mechanism of TLU under the System-Level ESD Test -- Component-Level Measurement for TLU under System-Level ESD Considerations -- TLU Dependency on Power-Pin Damping Frequency and Damping Factor in CMOS Integrated Circuits -- TLU in CMOS ICs in the Electrical Fast Transient Test -- Methodology on Extracting Compact Layout Rules for Latchup Prevention -- Special Layout Issues for Latchup Prevention -- TLU Prevention in Power-Rail ESD Clamp Circuits -- Appendix A: Practical Application Extractions of Latchup Design Rules in a 0.18-mm 1.8 V/3.3V Silicided CMOS Process.
Sommario/riassunto	"Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient

component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process."--Publisher's description.