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Sommario/riassunto	Designing aliasing-free space support hardware for built-in self-testing in very large scale integration circuits and systems is of immense significance, specifically due to the design paradigm shift in recent years from system-on-board to system-on-chip. This paper develops an approach to designing aliasing-free space compaction hardware targeting particularly embedded cores-based system-on-chips for single stuck-line faults, extending well known concept from conventional switching theory, viz. that of compatibility relation as used in the minimization of incompletely specified sequential machines. For a pair of response outputs of the circuit under test, the method introduces the notion of fault detection compatibility and conditional fault detection compatibility (conditional upon some other response output pair being simultaneously fault detection compatible) with respect to two-input OR/NOR logic. The process is illustrated with design details of space compactors for the International Symposium on Circuits and Systems or ISCAS 85 combinational (and ISCAS 89 full-scan sequential) benchmark circuits using simulation programs ATALANTA and FSIM, attesting to the importance of the technique from the viewpoint simplicity, resultant low area overhead and full fault coverage for single stuck-line faults, thereby making it an appropriate choice in commercial design environments.