1. Record Nr. UNINA9910139111803321

Titolo	Handbook of 3D integration . Volume 3 3D process technology / / edited by Philip Garrou, Mitsumasa Koyanagi, and Peter Ramm ; Richard A. Allen [and sixty others], contributors
Pubbl/distr/stampa	Weinheim, Germany : , : Wiley-VCH, , 2014 ©2014
ISBN	3-527-67012-2 3-527-67010-6 3-527-67013-0
Descrizione fisica	1 online resource (475 p.)
Disciplina	621.3815
Soggetti	Integrated circuits Integrated circuits - Design and construction Silicon Three-dimensional imaging
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references at the end of each chapters and index.
Nota di contenuto	Handbook of 3D Integration: 3D Process Technology; Contents; List of Contributors; 1 3D IC Integration Since 2008; 1.1 3D IC Nomenclature; 1.2 Process Standardization; 1.3 The Introduction of Interposers (2.5D); 1.4 The Foundries; 1.4.1 TSMC; 1.4.2 UMC; 1.4.3 GlobalFoundries; 1.5 Memory; 1.5.1 Samsung; 1.5.2 Micron; 1.5.3 Hynix; 1.6 The Assembly and Test Houses; 1.7 3D IC Application Roadmaps; References; 2 Key Applications and Market Trends for 3D Integration and Interposer Technologies; 2.1 Introduction; 2.2 Advanced Packaging Importance in the Semiconductor Industry is Growing 2.3 3D Integration-Focused Activities - The Global IP Landscape2.4 Applications, Technology, and Market Trends; References; 3 Economic Drivers and Impediments for 2.5D/3D Integration; 3.1 3D Performance Advantages; 3.2 The Economics of Scaling; 3.3 The Cost of Future Scaling; 3.4 Cost Remains the Impediment to 2.5D and 3D Product Introduction; 3.4.1 Required Economics for Interposer Use in Mobile

Products; 3.4.2 Silicon Interposer Pricing; References; 4 Interposer Technology; 4.1 Definition of 2.5D Interposers; 4.2 Interposer Drivers and Need; 4.3 Comparison of Interposer Materials
4.4 Silicon Interposers with TSV4.5 Lower Cost Interposers; 4.5.1 Glass Interposers; 4.5.1.1 Challenges in Glass Interposers; 4.5.1.2 Small-Pitch Through-Package Via Hole Formation and Ultrathin Glass Handling; 4.5.1.3 Metallization of Glass TPV; 4.5.1.4 Reliability of Copper TPVs in Glass Interposers; 4.5.1.5 Thermal Dissipation of Glass; 4.5.1.6 Glass Interposer Fabrication with TPV and RDL; 4.5.2 Low-CTE Organic Interposers; 4.5.3 Polycrystalline Silicon Interposer; 4.5.3.1 Polycrystalline Silicon Interposer Fabrication Process; 4.6 Interposer Technical and Manufacturing Challenges
4.7 Interposer Application Examples4.8 Conclusions; References; 5 TSV Formation Overview; 5.1 Introduction; 5.2 TSV Process Approaches; 5.2.1 TSV-Middle Approach; 5.2.2 Backside TSV-Last Approach; 5.2.3 Front-Side TSV-Last Approach; 5.3 TSV Fabrication Steps; 5.3.1 TSV Etching; 5.3.2 TSV Insulation; 5.3.3 TSV Metallization; 5.3.4 Overburden Removal by CMP; 5.3.5 TSV Anneal; 5.3.6 Temporary Carrier Wafer Bonding and Debonding; 5.3.7 Wafer Thinning and TSV Reveal; 5.4 Yield and Reliability; References; 6 TSV Unit Processes and Integration; 6.1 Introduction; 6.2 TSV Process Overview
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6.7 Integration with Packaging

Sommario/riassunto

Edited by key figures in 3D integration and written by top authors from high-tech companies and renowned research institutions, this book covers the intricate details of 3D process technology.As such, the main focus is on silicon via formation, bonding and debonding, thinning, via reveal and backside processing, both from a technological and a materials science perspective. The last part of the book is concerned with assessing and enhancing the reliability of the 3D integrated devices, which is a prerequisite for the large-scale implementation of this emerging technology. Invaluable re