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Sommario/riassunto	Low-power test aims at reduction of power-induced effects in the circuit under test in order to prevent overtesting. In contrast, noise-aware test attempts to maximize power noise to excite the chip in worst-case situations. Does low-power test potentially lead to test escapes? Will noise-aware test sort out chips which would never fail in their actual operation? What is the right approach, or the right mix of the approaches? Is the academia working on the right problems? This panel brings together experts from academia, semiconductor, EDA and IP industry.