

1. Record Nr.	UNINA9910139089603321
Autore	Chu Pong P. <1959->
Titolo	Embedded SoPC design with NIOS II processor and Verilog examples [[electronic resource] /] / Pong P. Chu
Pubbl/distr/stampa	Hoboken, N.J., : Wiley, c2012
ISBN	1-280-59239-7 9786613622228 1-118-30957-X 1-118-30972-3 1-118-30946-4
Edizione	[1st edition]
Descrizione fisica	1 online resource (783 p.)
Classificazione	TEC008010
Disciplina	006.2/2
Soggetti	Embedded computer systems Field programmable gate arrays Verilog (Computer hardware description language)
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	pt. I. Basic digital circuits development -- pt. II. Basic NIOS II software development -- pt. III. Custom I/O peripheral development -- pt. IV. Hardware accelerator case studies.
Sommario/riassunto	"This book explores the unique hardware programmability of FPGA (field-programmable gate array)-based embedded systems, using a learning-by-doing approach to introduce the concepts and techniques for embedded SoPC (system on a programmable chip) systems with Verilog. The book contains a large number of practical examples to illustrate and reinforce the hardware and software design concepts and techniques, as well as a complete code listing and experiment problems. The book is designed for upper-level undergraduate and entry-level graduate students in computer engineering, as well as practicing engineers"--