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Autore	Voldman Steven H
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Nota di contenuto	Electrical Overstress (EOS): Devices, Circuits and Systems; Contents; About the Author; Preface; Acknowledgements; 1 Fundamentals of Electrical Overstress; 1.1 Electrical Overstress; 1.1.1 The Cost of Electrical Overstress; 1.1.2 Product Field Returns - The Percentage that is Electrical Overstress; 1.1.3 Product Field Returns - No Defect Found versus Electrical Overstress; 1.1.4 Product Failures - Failures in Integrated Circuits; 1.1.5 Classification of Electrical Overstress Events; 1.1.6 Electrical Over-Current; 1.1.7 Electrical Over-Voltage; 1.1.8 Electrical Over-Power 1.2 De-Mystifying Electrical Overstress1.2.1 Electrical Overstress Events; 1.3 Sources of Electrical Overstress; 1.3.1 Sources of Electrical Overstress in Manufacturing Environment; 1.3.2 Sources of Electrical Overstress in Production Environments; 1.4 Misconceptions of Electrical Overstress; 1.5 Minimization of Electrical Overstress Sources; 1.6 Mitigation of Electrical Overstress; 1.7 Signs of Electrical Overstress Damage; 1.7.1 Signs of Electrical Overstress Damage - The Electrical Signature; 1.7.2 Signs of Electrical Overstress Damage - The Visual Signature

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1.11.2 Temperature Dependent Electrical Overstress1.11.3 Electrical Overstress and Melting Temperature; 1.12 Reliability Technology Scaling; 1.12.1 Reliability Technology Scaling and the Reliability Bathtub Curve; 1.12.2 The Shrinking Reliability Design Box; 1.12.3 The Shrinking Electrostatic Discharge Design Box; 1.12.4 Application Voltage, Trigger Voltage, and Absolute Maximum Voltage; 1.13 Safe Operating Area; 1.13.1 Electrical Safe Operating Area; 1.13.2 Thermal Safe Operating Area; 1.13.3 Transient Safe Operating Area; 1.14 Summary and Closing Comments; References
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2.2.7 The Cable Discharge Event Pulse Time Constant

Sommario/riassunto

"Electrical Overstress (EOS) continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-electronics. This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures. The text provides a clear picture of EOS phenomena, EOS origins, EOS sources, EOS physics, EOS failure mechanisms, and EOS on-chip and system design. It provides an illuminating insight into the sources of EOS in manufacturing, integration of on-chip, and system level EOS protection networks, followed by examples in specific technologies, circuits, and chips. The book is unique in covering the EOS manufacturing issues from on-chip design and electronic design automation to factory-level EOS program management in today's modern world.Look inside for extensive coverage on: Fundamentals of electrical overstress, from EOS physics, EOS time scales, safe operating area (SOA), to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment, and EOS program management, handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices, circuits and system Discussion of how to distinguish between EOS events, and electrostatic discharge (ESD) events (e.g. such as human body model (HBM), charged device model (CDM), cable discharge events (CDM), charged board events (CBE), to system level IEC 61000-4-2 test events) EOS protection on-chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards (PCB), and manufacturing equipment Examples of EOS issues in state-of-the-art digital, analog and power technologies including CMOS, LDMOS, and BCD EOS design rule checking (DRC), LVS, and ERC electronic design automation (EDA) and how it is distinct from ESD EDA systems EOS testing and qualification techniques, and Practical off-chip

ESD protection and system level solutions to provide more robust systems Electrical Overstress (EOS): Devices, Circuits and Systems is a continuation of the author's series of books on ESD protection. It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano-electronic era"--