

1. Record Nr.	UNINA9910136953103321
Titolo	Abiotic and Biotic Stress in Plants a : Recent Advances and Future Perspectives // edited by Arun K. Shanker and Chitra Shanker
Pubbl/distr/stampa	Rijeka : , : IntechOpen, , 2016 ©2016
ISBN	953-51-4209-7 953-51-2250-9
Edizione	[First edition.]
Descrizione fisica	1 online resource (768 pages) : illustrations
Disciplina	613.2
Soggetti	Nutrition
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references.
Sommario/riassunto	The impact of global climate change on crop production has emerged as a major research priority during the past decade. Understanding abiotic stress factors such as temperature and drought tolerance and biotic stress tolerance traits such as insect pest and pathogen resistance in combination with high yield in plants is of paramount importance to counter climate change related adverse effects on the productivity of crops. In this multi-authored book, we present synthesis of information for developing strategies to combat plant stress. Our effort here is to present a judicious mixture of basic as well as applied research outlooks so as to interest workers in all areas of plant science. We trust that the information covered in this book would bridge the much-researched area of stress in plants with the much-needed information for evolving climate-ready crop cultivars to ensure food security in the future.

2. Record Nr.	UNINA9910349358003321
Titolo	62142-2005 - IEC/IEEE International standard - Verilog(R) Register Transfer Level synthesis // Institute of Electrical and Electronics Engineers
Pubbl/distr/stampa	New York, New York : , : IEEE, , 2002
ISBN	0-7381-4777-X
Descrizione fisica	1 online resource (116 pages)
Disciplina	621.392
Soggetti	VHDL (Computer hardware description language)
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Sommario/riassunto	Replaces IEEE Std 1364.1-2002. To develop a standard syntax and semantics for Verilog RTL synthesis. This standard shall define the subset of IEEE 1364 (Verilog HDL) which is suitable for RTL synthesis and shall define the semantics of that subset for the synthesis domain. This standard shall be based on the current existing standard IEEE 1364.