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Titolo	Designing with Xilinx® FPGAs : Using Vivado / / edited by Sanjay Churiwala
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ISBN	3-319-42438-6
Edizione	[1st ed. 2017.]
Descrizione fisica	1 online resource (X, 260 p. 141 illus., 3 illus. in color.)
Disciplina	621.3815
Soggetti	Electronic circuits Microprocessors Electronics Microelectronics Circuits and Systems Processor Architectures Electronics and Microelectronics, Instrumentation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	State of the Art Programmable Logic -- Vivado Design Tools -- IP Flows -- Gigabit Transceivers -- Memory Controllers -- Processor Options -- Vivado IP Integrator -- SysGen for DSP -- Synthesis -- C Based Design -- Simulation -- Clocking -- Stacked Silicon Interconnect -- Timing Closure -- Power Analysis and Optimization -- System Monitor -- Hardware Debug -- Emulation Using FPGAs -- Partial Reconfiguration & Hierarchical Design.
Sommario/riassunto	This book helps readers to implement their designs on Xilinx® FPGAs. The authors demonstrate how to get the greatest impact from using the Vivado® Design Suite, which delivers a SoC-strength, IP-centric and system-centric, next generation development environment that has been built from the ground up to address the productivity bottlenecks in system-level integration and implementation. This book is a hands-on guide for both users who are new to FPGA designs, as well as those currently using the legacy Xilinx tool set (ISE) but are now moving to Vivado. Throughout the presentation, the authors focus on key

concepts, major mechanisms for design entry, and methods to realize the most efficient implementation of the target design, with the least number of iterations.