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   Sommario/riassunto   The current interpretation of common logic values and the association
                                     of numeric values to specific VHDL array types is described. This
                                     standard provides semantic for the VHDL synthesis domain, and
                                     enables formal verification and simulation acceleration in the VHDL
                                     based design. The standard interpretations are provided for values of
                                     standard logic types defined by IEEE Std 1164-1993, and of the BIT and
                                     BOOLEAN types defined in IEEE Std 1076-1993. The numeric types
                                     SIGNED and UNSIGNED and their associated operators define integer
                                     and natural number arithmetic for arrays of common logic values. Twos
                                     complement and binary encoding techniques are used. The numeric
                                     semantic is conveyed by two VHDL packages. This standard also
                                     contains any allowable modifications.