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Nota di contenuto	Cover; Title Page; Copyright; Contents; Introduction; Part 1. Prolog: Optimizing Compilation; Chapter 1. On The Decidability Of Phase Ordering In Optimizing Compilation; 1.1. Introduction to the phase ordering problem; 1.2. Background on phase ordering; 1.2.1. Performance modeling and prediction; 1.2.2. Some attempts in phase ordering; 1.3. Toward a theoretical model for the phase ordering problem; 1.3.1. Decidability results; 1.3.2. Another formulation of the phase ordering problem; 1.4. Examples of decidable simplified cases; 1.4.1. Models with compilation costs 1.4.2. One-pass generative compilers1.5. Compiler optimization parameter space exploration; 1.5.1. Toward a theoretical model; 1.5.2. Examples of simplified decidable cases; 1.6. Conclusion on phase ordering in optimizing compilation; Part 2. Instruction Scheduling; Chapter 2. Instruction Scheduling Problems And Overview; 2.1. VLIW instruction scheduling problems; 2.1.1. Instruction scheduling and register allocation in a code generator; 2.1.2. The block and pipeline VLIW instruction scheduling problems; 2.2. Software pipelining; 2.2.1. Cyclic, periodic and pipeline scheduling problems 2.2.2. Modulo instruction scheduling problems and techniques2.3. Instruction scheduling and register allocation; 2.3.1. Register instruction scheduling problem solving approaches; Chapter 3.

Applications Of Machine Scheduling To Instruction Scheduling; 3.1. Advances in machine scheduling; 3.1.1. Parallel machine scheduling problems; 3.1.2. Parallel machine scheduling extensions and relaxations; 3.2. List scheduling algorithms; 3.2.1. List scheduling algorithms and list scheduling priorities; 3.2.2. The scheduling algorithm of Leung, Palem and Pnueli
3.3. Time-indexed scheduling problem formulations
3.3.1. The non-preemptive time-indexed RCPSP formulation; 3.3.2. Time-indexed formulation for the modulo RPISP; Chapter 4. Instruction Scheduling Before Register Allocation; 4.1. Instruction scheduling for an ILP processor: case of a VLIW architecture; 4.1.1. Minimum cumulative register lifetime modulo scheduling; 4.1.2. Resource modeling in instruction scheduling problems; 4.1.3. The modulo insertion scheduling theorems; 4.1.4. Insertion scheduling in a backend compiler
4.1.5. Example of an industrial production compiler from STMicroelectronics
4.1.6. Time-indexed formulation of the modulo RCISP; 4.2. Large neighborhood search for the resource-constrained modulo scheduling problem; 4.3. Resource-constrained modulo scheduling problem; 4.3.1. Resource-constrained cyclic scheduling problems; 4.3.2. Resource-constrained modulo scheduling problem statement; 4.3.3. Solving resource-constrained modulo scheduling problems; 4.4. Time-indexed integer programming formulations; 4.4.1. The non-preemptive time-indexed RCPSP formulation
4.4.2. The classic modulo scheduling integer programming formulation

Sommario/riassunto

This book is a summary of more than a decade of research in the area of backend optimization. It contains the latest fundamental research results in this field. While existing books are often more oriented toward Masters students, this book is aimed more towards professors and researchers as it contains more advanced subjects. It is unique in the sense that it contains information that has not previously been covered by other books in the field, with chapters on phase ordering in optimizing compilation; register saturation in instruction level parallelism; code size reduction for softw
