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Nota di contenuto	Cover; Table of Contents; Title Page; Copyright; List of Figures; List of Tables; Preface; Chapter 1: Computer Fundamentals and Performance Evaluation; 1.1 Overview of Computer Systems; 1.2 Basic Structure of Computers; 1.3 Improving Computer Performance; 1.4 Hardware Description Languages; Exercises; Chapter 2: A Brief Introduction to Logic Circuits and Verilog HDL; 2.1 Logic Gates; 2.2 Logic Circuit Design in Verilog HDL; 2.3 CMOS Logic Gates; 2.4 Four Levels/Styles of Verilog HDL; 2.5 Combinational Circuit Design; 2.6 Sequential Circuit Design; Exercises Chapter 3: Computer Arithmetic Algorithms and Implementations3.1 Binary Integers; 3.2 Binary Addition and Subtraction; 3.3 Binary Multiplication Algorithms; 3.4 Binary Division Algorithms; 3.5 Binary Square Root Algorithms; Exercises; Chapter 4: Instruction Set Architecture and ALU Design; 4.1 Instruction Set Architecture; 4.2 MIPS Instruction Format and Registers; 4.3 MIPS Instructions and AsmSim Tool; 4.4 ALU Design; Exercises; Chapter 5: Single-Cycle CPU Design in Verilog HDL; 5.1 The Circuits Required for Executing an Instruction; 5.2 Register File Design 5.3 Single-Cycle CPU Datapath Design5.4 Single-Cycle CPU Control

Unit Design; 5.5 Test Program and Simulation Waveform; Exercises; Chapter 6: Exceptions and Interrupts Handling and Design in Verilog HDL; 6.1 Exceptions and Interrupts; 6.2 Design of CPU with Exception and Interrupt Mechanism; 6.3 The CPU Exception and Interrupt Tests; Exercises; Chapter 7: Multiple-Cycle CPU Design in Verilog HDL; 7.1 Dividing Instruction Execution into Several Clock Cycles; 7.2 Multiple-Cycle CPU Schematic and Verilog HDL Codes; 7.3 Multiple-Cycle CPU Control Unit Design; 7.4 Memory and Test Program Exercises; Chapter 8: Design of Pipelined CPU with Precise Interrupt in Verilog HDL; 8.1 Pipelining; 8.2 Pipeline Hazards and Solutions; 8.3 The Circuit of the Pipelined CPU and Verilog HDL Codes; 8.4 Precise Interrupts/Exceptions in Pipelined CPU; 8.5 Design of Pipelined CPU with Precise Interrupt/Exception; Exercises; Chapter 9: Floating-Point Algorithms and FPU Design in Verilog HDL; 9.1 IEEE 754 Floating-Point Data Formats; 9.2 Converting between Floating-Point Number and Integer; 9.3 Floating-Point Adder (FADD) Design; 9.4 Floating-Point Multiplier (FMUL) Design; 9.5 Floating-Point Divider (FDIV) Design; 9.6 Floating-Point Square Root (FSQRT) Design; Exercises; Chapter 10: Design of Pipelined CPU with FPU in Verilog HDL; 10.1 CPU/FPU Pipeline Model; 10.2 Design of Register File with Two Write Ports; 10.3 Data Dependency and Pipeline Stalls; 10.4 Pipelined CPU/FPU Design in Verilog HDL; 10.5 Memory Modules and Pipelined CPU/FPU Test; Exercises; Chapter 11: Memory Hierarchy and Virtual Memory Management; 11.1 Memory; 11.2 Cache Memory; 11.3 Virtual Memory Management and TLB Design; 11.4 Mechanism of TLB-Based MIPS Memory Management; Exercises; Chapter 12: Design of Pipelined CPU with Caches and TLBs in Verilog HDL

Sommario/riassunto

Uses Verilog HDL to illustrate computer architecture and microprocessor design, allowing readers to readily simulate and adjust the operation of each design, and thus build industrially relevant skills. Introduces the computer principles, computer design, and how to use Verilog HDL (Hardware Description Language) to implement the design. Provides the skills for designing processor/arithmetic/cpu chips, including the unique application of Verilog HDL material for CPU (central processing unit) implementation. Despite the many books on Verilog and computer architecture and microprocessor design, few

2. Record Nr.	UNINA9910286454103321
Autore	Yáñez Agustín
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Pubbl/distr/stampa	El Colegio de México, 1992 Mexico, D.F. : , : Colegio de Mexico, , 1992 ©1992
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Collana	Lecturas de "Historia Mexicana" ; ; 3
Altri autori (Persone)	YanezAgustin <1904-1980.> FalconRamona
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Soggetti	History of the Americas Mexico History
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Nota di bibliografia	Includes bibliographical references.
Sommario/riassunto	Esta selección ofrece un recorrido por el tiempo de nuestro pasado y de nuestra historiografía, que muestra ejemplos sobresalientes de dos temas íntimamente relacionados, y en los que esta revista tradicionalmente ha hecho hincapié. El primero se refiere a la enorme diversidad de actores políticos y el segundo campo se centra en algunas aristas de los grandes problemas y movimientos sociales que hilvanaron la historia de México a lo largo del siglo XIX y la revolución iniciada en 1910.