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1.6 ESD TESTING1.6.1 ESD Qualification Testing; 1.6.2 ESD Test Models; 1.6.3 ESD Characterization Testing; 1.6.4 TLP Testing; 1.7 ESD CHIP ARCHITECTURE AND ESD ALTERNATIVE CURRENT PATHS; 1.7.1 ESD Circuits, I/O, and Cores; 1.7.2 ESD Signal Pin Circuits; 1.7.3 ESD Power Clamp Networks; 1.7.4 ESD Rail-to-Rail Circuits; 1.7.5 ESD Design and Noise; 1.7.6 Internal Signal Path ESD Networks; 1.7.7 Cross-Domain ESD Networks; 1.8 ESD NETWORKS, SEQUENCING, AND CHIP ARCHITECTURE; 1.9 ESD DESIGN SYNTHESIS - LATCHUP-FREE ESD NETWORKS; 1.10 ESD DESIGN CONCEPTS - BUFFERING - INTER-DEVICE 1.11 ESD DESIGN CONCEPTS - BALLASTING - INTER-DEVICE1.12 ESD DESIGN CONCEPTS - BALLASTING - INTRA-DEVICE; 1.13 ESD DESIGN CONCEPTS - DISTRIBUTED LOAD TECHNIQUES; 1.14 ESD DESIGN CONCEPTS - DUMMY CIRCUITS; 1.15 ESD DESIGN CONCEPTS - POWER SUPPLY DE-COUPLING; 1.16 ESD DESIGN CONCEPTS - FEEDBACK LOOP DE-COUPLING; 1.17 ESD LAYOUT AND FLOORPLAN-RELATED CONCEPTS; 1.17.1 Design Symmetry; 1.17.2 Design Segmentation; 1.17.3 ESD Design Concepts - Utilization of Empty Space; 1.17.4 ESD Design Synthesis - Across Chip Line Width Variation (ACLV); 1.17.5 ESD Design Concepts - Dummy Shapes
1.17.6 ESD Design Concepts - Dummy Masks1.17.7 ESD Design Concepts - Adjacency; 1.18 ESD DESIGN CONCEPTS - ANALOG CIRCUIT TECHNIQUES; 1.19 ESD DESIGN CONCEPTS - WIRE BONDS; 1.20 DESIGN RULES; 1.20.1 ESD Design Rule Checking (DRC); 1.20.2 ESD Layout vs. Schematic (LVS); 1.20.3 Electrical Resistance Checking (ERC); 1.21 SUMMARY AND CLOSING COMMENTS; PROBLEMS; REFERENCES; 2 ESD Architecture and Floorplanning; 2.1 ESD DESIGN FLOORPLAN; 2.2 PERIPHERAL I/O DESIGN; 2.2.1 Pad-Limited Peripheral I/O Design Architecture; 2.2.2 Pad-Limited Peripheral I/O Design Architecture - Staggered I/O
2.2.3 Core-Limited Peripheral I/O Design Architecture

Sommario/riassunto

Electrostatic discharge (ESD) continues to impact semiconductor components and systems as technologies scale from micro- to nano-electronics. This book studies electrical overstress, ESD, and latchup from a whole-chip ESD design synthesis approach. It provides a clear insight into the integration of ESD protection networks from a generalist perspective, followed by examples in specific technologies, circuits, and chips. Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a 'top-down' design approach. Look inside for extensive coverage