1. Record Nr. UNINA990008016320403321

Autore	Liebeschuetz, John Hugo Wolfgang Gideon
Titolo	Barbarians and bishops : Army, church, and state in the age of Arcadius and Chrysostom / J.H.W.G. Liebeschuetz
Pubbl/distr/stampa	Oxford : Clarendon Press, 1990
ISBN	0-19-814073-8
Descrizione fisica	XIV, 312 p., [4]c. di tav. : ill. ; 24 cm
Locazione	DDR
Collocazione	DDR-XX Db 010
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA9911006647203321

Autore	Lilja David J
Titolo	Designing digital computing systems with Verilog / / David J. Lilja and Sachin S. Sapatnekar
Pubbl/distr/stampa	Cambridge ; ; New York, : Cambridge University Press, 2005
ISBN	1-107-16031-6 1-280-74962-8 9786610749621 0-511-26247-7 0-511-26486-0 0-511-26558-1 0-511-26328-7 0-511-33160-6 0-511-60705-9 0-511-26409-7
Descrizione fisica	1 online resource (ix, 160 pages) : digital, PDF file(s)
Altri autori (Persone)	SapatnekarSachin S. <1967->
Disciplina	621.39/2
Soggetti	Verilog (Computer hardware description language) Electronic digital computers - Design and construction

Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Title from publisher's bibliographic system (viewed on 05 Oct 2015).
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Cover; Half-title; Title; Copyright; Contents; Preface; 1 Controlling complexity; 2 A Verilogical place to start; 3 Defining the instruction set architecture; 4 Algorithmic behavioral modeling; 5 Building an assembler for VeSPA; 6 Pipelining; 7 Implementation of the pipelined processor; 8 Verification; APPENDIX A The VeSPA instruction set architecture (ISA); APPENDIX B The VASM assembler; Index
Sommario/riassunto	This book serves both as an introduction to computer architecture and as a guide to using a hardware description language (HDL) to design, model and simulate real digital systems. The book starts with an introduction to Verilog - the HDL chosen for the book since it is widely used in industry and straightforward to learn. Next, the instruction set architecture (ISA) for the simple VeSPA (Very Small Processor Architecture) processor is defined - this is a real working device that has been built and tested at the University of Minnesota by the authors. The VeSPA ISA is used throughout the remainder of the book to demonstrate how behavioural and structural models can be developed and intermingled in Verilog. Although Verilog is used throughout, the lessons learned will be equally applicable to other HDLs. Written for senior and graduate students, this book is also an ideal introduction to Verilog for practising engineers.