1. Record Nr. UNINA990007578190403321

Autore	Capitani, Giancarlo
Titolo	Industrializzazione e terziarizzazione diffusa in Lombardia / G. Capitani, G. Garofoli
Descrizione fisica	p. 119-148 : ill.
Altri autori (Persone)	Garofoli, Gioacchino
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA990007009020403321

Titolo	Libistro e Rodamne : romanzo cavalleresco bizantino ; introduzione e versione italiana di Vincenzo Rotolo
Pubbl/distr/stampa	Atene : Aohnai, 1965
Descrizione fisica	60 p. ; 20 cm
Locazione	BAT
Collocazione	BIB. BAT.5353
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
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3. Record Nr. UNINA9911002557203321

Autore	Ortega Cisneros Susana
Titolo	Integrated Circuit Design : Tape-out Process with Open-Source Tools / / by Susana Ortega Cisneros, Emilio Isaac Baungarten Leon, Pedro Mejia Alvarez
Pubbl/distr/stampa	Cham : , : Springer Nature Switzerland : , : Imprint : Springer, , 2025
ISBN	9783031921087 9783031921070
Edizione	[1st ed. 2025.]
Descrizione fisica	1 online resource (118 pages)
Collana	SpringerBriefs in Computer Science, , 2191-5776
Altri autori (Persone)	Baungarten LeonEmilio Isaac Mejia AlvarezPedro
Disciplina	004.22
Soggetti	Microprocessors Computer architecture Electronic circuits Open source software Processor Architectures Electronic Circuits and Systems Open Source
Lingua di pubblicazione	Inglese
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Nota di contenuto	1: Introduction -- 2: Physical Design Flow -- 3: Process Design Kit -- 4: Introduction to OpenLane -- 5: Macro-Cells and RAM-Cells with OpenLane -- 6: Exploring OpenLane through Case Studies and Exercises -- 7: Caravel.
Sommario/riassunto	This book provides a structured and comprehensive pathway through the complexities of Electronic Design Automation (EDA) tools and processes. It focuses on OpenLane and Caravel EDA tools, due to their current major role in the open-source IC design ecosystem. OpenLane provides a robust and flexible platform that automates the entire digital design flow from Register Transfer Level (RTL) to Graphic Data System II (GDSII), making it an ideal tool for teaching and learning the physical design process. Caravel, on the other hand, serves as an open-source System on a Chip (SoC) platform, allowing designers to integrate

and test their designs in a versatile, real-world environment. It complements OpenLane by enabling users to package and validate their designs, bridging the gap between theoretical knowledge and practical implementation. Together, these tools provide a way to understand the full tape-out process in a way that is accessible to students, researchers, and professionals alike.