

1. Record Nr.	UNINA990007490420403321
Autore	Martonne, Emmanuel de <1873-1955>
Titolo	Traité de géographie physique / Emm. de Martonne
Pubbl/distr/stampa	Paris : Colin, 1925-1929
Edizione	[4e édition entièrement refondue]
Descrizione fisica	3 v. (XI; XIII, 1518 p.) : ill. ; 25 cm
Disciplina	030.001 910 912 581.9
Locazione	ILFGE FINBC DECGE
Collocazione	B-03-047 B-03-046 B-03-045 13 L 43 43 13 L 43 41 13 L 43 42 13 L 43 44 13 L 43 45 030.001.MAR.02
Lingua di pubblicazione	Francese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di contenuto	1.: Notions générales, climat, hydrographie. - 1925 2.: Le relief du sol. - 1926 3.: Biogéographie, avec la collaboration de Aug. Chevalier, L. Cuénot. - 1929

2. Record Nr.	UNINA9910456662303321
Autore	Yiu Joseph
Titolo	The definitive guide to the ARM Cortex-M3 [[electronic resource] /] / Joseph Yiu
Pubbl/distr/stampa	Amsterdam ; ; Boston, : Newnes, c2010
ISBN	1-282-75584-6 9786612755842 1-85617-964-8
Edizione	[2nd ed.]
Descrizione fisica	1 online resource (481 p.)
Disciplina	621.39/16
Soggetti	Embedded computer systems Microprocessors Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Front Cover; Half Title Page; The Definitive Guide to the ARM Cortex-M3; Copyright Page; Table of Contents; Foreword; Foreword; Preface; Acknowledgments; Conventions; Terms and Abbreviations; Chapter 1. Introduction; 1.1 What Is the ARM Cortex-M3 Processor?; 1.2 Background of ARM and ARM Architecture; 1.2.1 A Brief History; 1.2.2 Architecture Versions; 1.2.3 Processor Naming; 1.3 Instruction Set Development; 1.4 The Thumb-2 Technology and Instruction Set Architecture; 1.5 Cortex-M3 Processor Applications; 1.6 Organization of This Book; 1.7 Further Reading; Chapter 2. Overview of the Cortex-M3 2.1 Fundamentals2.2 Registers; 2.2.1 R0-R12: General-Purpose Registers; 2.2.2 R13: Stack Pointers; 2.2.3 R14: The Link Register; 2.2.4 R15: The Program Counter; 2.2.5 Special Registers; 2.3 Operation Modes; 2.4 The Built-In Nested Vectored Interrupt Controller; 2.4.1 Nested Interrupt Support; 2.4.2 Vectored Interrupt Support; 2.4.3 Dynamic Priority Changes Support; 2.4.4 Reduction of Interrupt Latency; 2.4.5 Interrupt Masking; 2.5 The Memory Map; 2.6 The Bus Interface; 2.7 The MPU; 2.8 The Instruction Set; 2.9 Interrupts and Exceptions; 2.9.1 Low Power and High Energy Efficiency

2.10 Debugging Support; 2.11 Characteristics Summary; 2.11.1 High Performance; 2.11.2 Advanced Interrupt-Handling Features; 2.11.3 Low Power Consumption; 2.11.4 System Features; 2.11.5 Debug Supports; Chapter 3. Cortex-M3 Basics; 3.1 Registers; 3.1.1 General Purpose Registers R0 through R7; 3.1.2 General Purpose Registers R8 through R12; 3.1.3 Stack Pointer R13; 3.1.4 Link Register R14; 3.1.5 Program Counter R15; 3.2 Special Registers; 3.2.1 Program Status Registers; 3.2.2 PRIMASK, FAULTMASK, and BASEPRI Registers; 3.2.3 The Control Register; 3.3 Operation Mode; 3.4 Exceptions and Interrupts; 3.5 Vector Tables; 3.6 Stack Memory Operations; 3.6.1 Basic Operations of the Stack; 3.6.2 Cortex-M3 Stack Implementation; 3.6.3 The Two-Stack Model in the Cortex-M3; 3.7 Reset Sequence; Chapter 4. Instruction Sets; 4.1 Assembly Basics; 4.1.1 Assembler Language: Basic Syntax; 4.1.2 Assembler Language: Use of Suffixes; 4.1.3 Assembler Language: Unified Assembler Language; 4.2 Instruction List; 4.2.1 Unsupported Instructions; 4.3 Instruction Descriptions; 4.3.1 Assembler Language: Moving Data; 4.3.2 LDR and ADR Pseudo-Instructions; 4.3.3 Assembler Language: Processing Data; 4.3.4 Assembler Language: Call and Unconditional Branch; 4.3.5 Assembler Language: Decisions and Conditional Branches; 4.3.6 Assembler Language: Combined Compare and Conditional Branch; 4.3.7 Assembler Language: Instruction Barrier and Memory Barrier Instructions; 4.3.8 Assembly Language: Saturation Operations; 4.4 Several Useful Instructions in the Cortex-M3; 4.4.1 MSR and MRS; 4.4.2 More on the IF-THEN Instruction Block; 4.4.3 SDIV and UDIV; 4.4.4 REV, REVH, and REVSH; 4.4.5 Reverse Bit; 4.4.6 SXTB, SXTB, UXTB, and UXTB; 4.4.7 Bit Field Clear and Bit Field Insert; 4.4.8 UBFX and SBFX; 4.4.9 LDRD and STRD

Sommario/riassunto

This user's guide does far more than simply outline the ARM Cortex-M3 CPU features; it explains step-by-step how to program and implement the processor in real-world designs. It teaches readers how to utilize the complete and thumb instruction sets in order to obtain the best functionality, efficiency, and reuseability. The author, an ARM engineer who helped develop the core, provides many examples and diagrams that aid understanding. Quick reference appendices make locating specific details a snap! Whole chapters are dedicated to: Debugging using the new CoreSight technology
