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| 1. Record Nr. | UNINA990003304950403321 |
| Autore | De Beaugrande, Robert |
| Titolo | INTRODUCTION TO TEXT LINGUISTICO |
| Pubbl/distr/stampa | LONDON : LONGMAN, 1986 |
| Altri autori (Persone) | Dressler, Wolfgang U. <1939- > |
| Disciplina | 410 |
| Locazione | DECLI |
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| Lingua di pubblicazione | Italiano |
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| Livello bibliografico | Monografia |
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| 2. Record Nr. | UNISALENTO991001175119707536 |
| Titolo | La legge fallimentare dopo la riforma / a cura di Alessandro Nigro, Michele Sandulli e Vittorio Santoro |
| Pubbl/distr/stampa | Torino : Giappichelli, c2010 |
| ISBN | 9788834800164 (set) |
| Descrizione fisica | 3 v. (lxxxiii, 2567 p. compless.) ; 25 cm |
| Collana | Le nuove leggi del diritto dell'economia ; 11 |
| Altri autori (Persone) | Nigro, Alessandro
Sandulli, Michele
Santoro, Vittorio |
| Disciplina | 346.45078 |
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| Nota di contenuto | 1. Disposizioni generali, fallimento (artt. 1-83bis) -- 2. Fallimento (artt. 84-159) -- 3. Concordato preventivo e accordi di ristrutturazione, |

3. Record Nr.	UNINA9910760262603321
Autore	Rai Shubham
Titolo	Design Automation and Applications for Emerging Reconfigurable Nanotechnologies // by Shubham Rai, Akash Kumar
Pubbl/distr/stampa	Cham : , : Springer Nature Switzerland : , : Imprint : Springer, , 2024
ISBN	3-031-37924-1
Edizione	[1st ed. 2024.]
Descrizione fisica	1 online resource (230 pages)
Disciplina	006.3 621.3815
Soggetti	Electronic circuits Embedded computer systems Microprocessors Computer architecture Electronic Circuits and Systems Embedded Systems Processor Architectures
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Chapter 1. Introduction -- Chapter 2. Preliminaries -- Chapter 3. Exploring Circuit Design Topologies for RFETs -- Chapter 4. Standard Cells and Technology Mapping -- Chapter 5. Logic Synthesis with XOR-Majority Graphs -- Chapter 6. Physical synthesis flow and liberty generation -- Chapter 7. Polymorphic Primitives for Hardware Security -- Chapter 8. Conclusion.
Sommario/riassunto	This book is a single-source solution for anyone who is interested in exploring emerging reconfigurable nanotechnology at the circuit level. It lays down a solid foundation for circuits based on this technology having considered both manual as well as automated design flows. The authors discuss the entire design flow, consisting of both logic and physical synthesis for reconfigurable nanotechnology-based circuits. The authors describe how transistor reconfigurable properties can be exploited at the logic level to have a more efficient circuit design flow,

as compared to conventional design flows suited for CMOS. Further, the book provides insights into hardware security features that can be intrinsically developed using the runtime reconfigurable features of this nanotechnology. Details an entire design automation flow for building circuits based on emerging reconfigurable nanotechnology; Describes logical abstraction for emerging reconfigurable nanotechnology that is essential for building newer circuits; Presents hardware security solutions that use reconfigurable nanotechnology to complement contemporary CMOS circuits.
