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Nota di bibliografia

Includes bibliographical references at the end of each chapters.

Nota di contenuto

Chapter1. The Evolution of Software Defined Radio - An Introduction -- Part I: Architectures, Designs and Implementations -- Chapter2. Design Transformation from a Single-Core to a Multi-Core Architecture targeting Massively-Parallel Signal Processing Algorithms -- Chapter3. The CoreVA-MPSoC - A Multiprocessor Platform for Software-Defined Radio -- Chapter4. Design and Implementation of IEEE 802.11a/g Receiver Blocks on a Coarse-Grained Reconfigurable Array -- Chapter5. Recongurable Multiprocessor Systems-on-Chip -- Chapter6. NineSilica: A Homogeneous MPSoC approach for SDR platforms -- Part II: Software-based Radio Cognition and Implementation Tools -- Chapter7. Application of the Scalable Communications Core as an SDR Baseband -- Chapter8. HW/SW Co-Design Toolset for Customization of Exposed Datapath Processors -- Chapter9. FPGA-based Cognitive Radio Platform with Recongurable Front-End and Antenna -- Chapter10. Synchronization in NC-OFDM-Based CR Platforms -- Chapter11. Towards Adaptive Cryptography and Security with Software Dened Platforms -- Chapter12. The Future of Software-Defined Radio-Recommendations.

Sommario/riassunto

This book addresses Software-Defined Radio (SDR) baseband processing from the computer architecture point of view, providing a detailed exploration of different computing platforms by classifying different approaches, highlighting the common features related to SDR requirements and by showing pros and cons of the proposed solutions. Coverage includes architectures exploiting parallelism by extending single-processor environment (such as VLIW, SIMD, TTA approaches), multi-core platforms distributing the computation to either a homogeneous array or a set of specialized heterogeneous processors, and architectures exploiting fine-grained, coarse-grained, or hybrid reconfigurability. Describes a computer engineering approach to SDR baseband processing hardware; Discusses implementation of numerous compute-intensive signal processing algorithms on single and multicore platforms; Enables deep understanding of optimization techniques related to power and energy consumption of multicore platforms using several basic and high-level performance indicators; Includes prototyping details of single and multicore platforms on ASICs and FPGAs.