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Autore	Lee Weng Fook
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Nota di contenuto	Chapter 1. Introduction -- Chapter 2. Design Methodology and Flow -- Chapter 3. Multiple Clock Design -- Chapter 4. Latch Inference -- Chapter 5. Design for Test -- Chapter 6. Signed Verilog -- Chapter 7.

State Machine -- Chapter 8. RTL Coding Guideline -- Chapter 9. Code Coverage. .

Sommario/riassunto

This book shares with readers practical design knowledge gained from the author’s 24 years of IC design experience. The author addresses issues and challenges faced commonly by IC designers, along with solutions and workarounds. Guidelines are described for tackling issues such as clock domain crossing, using lockup latch to cross clock domains during scan shift, implementation of scan chains across power domain, optimization methods to improve timing, how standard cell libraries can aid in synthesis optimization, BKM (best known method) for RTL coding, test compression, memory BIST, usage of signed Verilog for design requiring +ve and -ve calculations, state machine, code coverage and much more. Numerous figures and examples are provided to aid the reader in understanding the issues and their workarounds. Addresses practical design issues and their workarounds; Discusses issues such as CDC, crossing clock domain in shift, scan chains across power domain, timing optimization, standard cell library influence on synthesis, DFT, code coverage, state machine; Provides readers with an RTL coding guideline, based on real experience.