1. Record Nr. UNICASSBL0341456

Titolo	La Bibbia di S. Paolo fuori le Mura : abbazia di S. Paolo fuori le Mura, Roma, 29 giugno-30 settembre 1981 / catalogo a cura di Viviana Jemolo e Mirella Morelli
Pubbl/distr/stampa	Roma, : De Luca, ©1981
Descrizione fisica	63 p. : ill. ; 24 cm
Disciplina	091
Soggetti	Codex paulinus - Roma - S. Paolo fuori le mura - Esposizioni Roma 1981
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	In testa al front.: Ministero per i beni culturali e ambientali, Ufficio centrale per i beni librari e gli istituti culturali; Istituto centrale per la patologia del libro, Roma.

2. Record Nr. UNINA9910144341103321

Titolo	Automated Technology for Verification and Analysis : Second International Conference, ATVA 2004, Taipei, Taiwan, ROC, October 31 - November 3, 2004. Proceedings / / edited by Farn Wang
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2004
ISBN	3-540-30476-2
Edizione	[1st ed. 2004.]
Descrizione fisica	1 online resource (XII, 510 p.)
Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 3299
Disciplina	004.015113
Soggetti	Computer-aided engineering Computer logic Computers Computer networks Computers, Special purpose Software engineering Computer-Aided Engineering (CAD, CAE) and Design Logics and Meanings of Programs Information Systems and Communication Service Computer Communication Networks Special Purpose and Application-Based Systems Software Engineering
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references at the end of each chapters and index.
Nota di contenuto	Keynote Speech -- Games for Formal Design and Verification of Reactive Systems -- Evolution of Model Checking into the EDA Industry -- Abstraction Refinement -- Invited Speech -- Tools for Automated Verification of Web Services -- Theorem Proving Languages for Verification -- An Automated Rigorous Review Method for Verifying and Validating Formal Specifications -- Papers -- Toward Unbounded Model Checking for Region Automata -- Search Space Partition and Case Basis Exploration for Reducing Model Checking Complexity -- Synthesising Attacks on Cryptographic Protocols -- Büchi

Complementation Made Tighter -- SAT-Based Verification of Safe Petri Nets -- Disjunctive Invariants for Numerical Systems -- Validity Checking for Quantifier-Free First-Order Logic with Equality Using Substitution of Boolean Formulas -- Fair Testing Revisited: A Process-Algebraic Characterisation of Conflicts -- Exploiting Symmetries for Testing Equivalence in the Spi Calculus -- Using Block-Local Atomicity to Detect Stale-Value Concurrency Errors -- Abstraction-Based Model Checking Using Heuristical Refinement -- A Global Timed Bisimulation Preserving Abstraction for Parametric Time-Interval Automata -- Design and Evaluation of a Symbolic and Abstraction-Based Model Checker -- Component-Wise Instruction-Cache Behavior Prediction -- Validating the Translation of an Industrial Optimizing Compiler -- Composition of Accelerations to Verify Infinite Heterogeneous Systems -- Hybrid System Verification Is Not a Sinecure -- Providing Automated Verification in HOL Using MDGs -- Specification, Abduction, and Proof -- Introducing Structural Dynamic Changes in Petri Nets: Marked-Controlled Reconfigurable Nets -- Typeness for ?-Regular Automata -- Partial Order Reduction for Detecting Safety and Timing Failures of Timed Circuits -- Mutation Coverage Estimation for Model Checking -- Modular Model Checking of Software Specifications with Simultaneous Environment Generation -- Rabin Tree and Its Application to Group Key Distribution -- Using Overlay Networks to Improve VoIP Reliability -- Integrity-Enhanced Verification Scheme for Software-Intensive Organizations -- RCGES: Retargetable Code Generation for Embedded Systems -- Verification of Analog and Mixed-Signal Circuits Using Timed Hybrid Petri Nets -- First-Order LTL Model Checking Using MDGs -- Localizing Errors in Counterexample with Iteratively Witness Searching -- Verification of WCDMA Protocols and Implementation -- Efficient Representation of Algebraic Expressions -- Development of RTOS for PLC Using Formal Methods -- Reducing Parametric Automata: A Multimedia Protocol Service Case Study -- Synthesis of State Feedback Controllers for Parameterized Discrete Event Systems -- Solving Box-Pushing Games via Model Checking with Optimizations -- CLP Based Static Property Checking -- A Temporal Assertion Extension to Verilog.

Sommario/riassunto

It was our great pleasure to hold the 2nd International Symposium onAutomated Te- nology on Veri?cation and Analysis (ATVA) in Taipei, Taiwan, ROC, October 31– November3,2004. TheseriesofATVAmeetingsisintendedforthepromotionofrelated research in eastern Asia. In the last decade, automated technology on veri?cation has become the new strength in industry and brought forward various hot research activities in both Europe and USA. In comparison, easternAsia has been quiet in the forum.With more and more IC design houses moving from SiliconValley to easternAsia, we believe this is a good time to start cultivating related research activities in the region. TheemphasisoftheATVAworkshopseriesisonvariousmechanicalandinfor mative techniques, which can give engineers valuable feedback to fast converge their designs according to the speci?cations. The scope of interest contains the following research - eas: model-checking theory, theorem-proving theory, state-space reduction techniques, languages in automated veri?cation, parametric analysis, optimization, formal perf- mance analysis, real-time systems, embedded systems, in?nite-state systems, Petri nets, UML, synthesis, tools, and practice in industry.