1. Record Nr. UNICASRML0269631

Autore	Jung, Carl Gustav
Titolo	10.2: Civiltà in transizione : dopo la catastrofe / Carl Gustav Jung ; [edizione diretta da Luigi Aurigemma]
Pubbl/distr/stampa	Torino, : P. Boringhieri, ©1986
Descrizione fisica	XI, 361 p., VIII p. di tav. : ill. ; 25 cm
Disciplina	302
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

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Autore	Bindal Ahmet
Titolo	Silicon Nanowire Transistors / / by Ahmet Bindal, Sotoudeh Hamedi-Hagh
Pubbl/distr/stampa	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2016
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Descrizione fisica	1 online resource (176 p.)
Disciplina	620
Soggetti	Electronic circuits Nanotechnology Circuits and Systems Electronic Circuits and Devices
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di contenuto	Dual Work Function Silicon Nanowire MOS Transistors -- Single Work Function Silicon Nanowire MOS Transistors -- Spice Modeling For Analog and Digital Applications -- High-Speed Analog Applications --

Radio Frequency (RF) Applications -- SRAM Mega Cell Design for Digital Applications -- Field-Programmable-Gate-Array (FPGA) -- Integrate-And-Fire Spiking (IFS) Neuron -- Direct Sequence Spread Spectrum (DSSS) Base-Band Transmitter.-.

Sommario/riassunto

This book describes the n and p-channel Silicon Nanowire Transistor (SNT) designs with single and dual-work functions, emphasizing low static and dynamic power consumption. The authors describe a process flow for fabrication and generate SPICE models for building various digital and analog circuits. These include an SRAM, a baseband spread spectrum transmitter, a neuron cell and a Field Programmable Gate Array (FPGA) platform in the digital domain, as well as high bandwidth single-stage and operational amplifiers, RF communication circuits in the analog domain, in order to show this technology's true potential for the next generation VLSI. Describes Silicon Nanowire (SNW) Transistors, as vertically constructed MOS n and p-channel transistors, with low static and dynamic power consumption and small layout footprint; Targets System-on-Chip (SoC) design, supporting very high transistor count (ULSI), minimal power consumption requiring inexpensive substrates for packaging; Enables fabrication of different types of memory on the same chip, such as capacitive cells and transistors with floating gates that can be used as DRAMs and Flash memories.