1. Record Nr. UNICASCAG0067385

Titolo	Indice generale
Pubbl/distr/stampa	Citta di Castello, : Unione arti grafiche, 1944
Descrizione fisica	98 p. ; 20 cm.
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia

2. Record Nr. UNINA9910746070903321

Titolo	Applied Reconfigurable Computing. Architectures, Tools, and Applications : 19th International Symposium, ARC 2023, Cottbus, Germany, September 27–29, 2023, Proceedings / / edited by Francesca Palumbo, Georgios Keramidas, Nikolaos Voros, Pedro C. Diniz
Pubbl/distr/stampa	Cham : , : Springer Nature Switzerland : , : Imprint : Springer, , 2023
ISBN	3-031-42921-4
Edizione	[1st ed. 2023.]
Descrizione fisica	1 online resource (380 pages)
Collana	Lecture Notes in Computer Science, , 1611-3349 ; ; 14251
Disciplina	004
Soggetti	Computers Computer engineering Computer networks Software engineering Computer Hardware Computer Engineering and Networks Software Engineering
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Design Methods and Tools -- High-Level Synthesis of Memory Systems for Decoupled Data Orchestration -- Rapid Prototyping of Complex

Micro-architectures through High-Level Synthesis -- NVMulator: A Con gurable Open-Source Non-Volatile Memory Emulator for FPGAs -- On the OpenCL Support for Streaming Fixed-Function Accelerators on Embedded SoC FPGAs -- Design Space Exploration of Application Specific Number Formats targeting an FPGA Implementation of SPICE -- Memory-Aware Scheduling for a Resource-Elastic FPGA Operating System -- ArcvaVX: OpenVX Framework for Adaptive Reconfigurable Computer Vision Architectures -- Applications -- FPGA-Integrated Bag of Little Bootstraps Accelerator for Approximate Database Query Processing -- Accelerating Graph Neural Networks in Pytorch With HLS and Deep Data flows -- DNN Model Theft through Trojan Side Channel on Edge FPGA Accelerator -- Towards Secure and Efficient Multi-generation Cellular Communications: Multi-mode SNOW-3G/V ASIC and FPGA Implementations -- A Convolution Neural Network based Displaced Vertex Trigger for the Belle II Experiment -- On-FPGA Spiking Neural Networks for Multi-Variable End-to-End Neural Decoding -- Implementation of a Perception System for Autonomous Vehicles using a Detection-Segmentation Network in SoC FPGA -- Architectures -- Increasing the Fault Tolerance of COTS FPGAs in Space: SEU Mitigation Techniques on MPSoC -- Scalable and Energy-Efficient NN Acceleration with GPU-ReRAM Architecture -- On Guaranteeing Schedulability of Periodic Real-time Hardware Tasks under ReconOS64 -- Evolutionary FPGA-based Spiking Neural Networks for Continual Learning -- More Efficient CMMs on FPGAs: Instantiated Ternary Adders for Computation Coding -- Energy Efficient DNN Compaction for Edge Deployment -- Special Session: Near and In-Memory Computing -- TAPRE-HBM: Trace-Based Processor Rapid Emulation using HBM on FPGAs -- An Almost Fully RRAM-based LUT Design for Reconfigurable Circuits -- A Light-weight Vision Transformer toward Near-Memory Computation on an FPGA -- PhD Forum Papers Radiation Tolerant Reconfigurable Hardware Architecture Design Methodology -- A Control Data Acquisition System Architecture for MPSoC-FPGAs in Computed Tomography -- Simulation and Modeling for Network-on-Chip based MPSoC -- A Design-Space Exploration Framework for Application-Specification -- Machine Learning targeting Reconfigurable Computing.

Sommario/riassunto

This book constitutes the proceedings of the 19th International Symposium on Applied Reconfigurable Computing, ARC 2023, which was held in Cottbus, Germany, in September 2023. The 18 full papers presented in this volume were reviewed and selected from numerous submissions. The proceedings also contain 4 short PhD papers. The contributions were organized in topical sections as follows: Design methods and tools; applications; architectures; special session: near and in-memory computing; and PhD forum papers. .