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Number Systems and Binary Codes; 1.1 Introduction; 1.2 Decimal Numbers; 1.3 Binary Numbers; 1.3.1 Basic Binary Arithmetic; 1.4 Octal Numbers; 1.5 Hexadecimal Numbers; 1.6 Signed Numbers; 1.6.1 Diminished Radix Complement; 1.6.2 Radix Complement; 1.7 Floating-Point Numbers; 1.8 Binary Encoding; 1.8.1 Weighted Codes; 1.8.2 Nonweighted Codes; Exercises; 2 Fundamental Concepts of Digital Logic; 2.1 Introduction; 2.2 Sets; 2.3 Relations; 2.4 Partitions; 2.5 Graphs; 2.6 Boolean Algebra; 2.7 Boolean Functions  
 2.8 Derivation and Classification of Boolean Functions 2.9 Canonical Forms of Boolean Functions; 2.10 Logic Gates; Exercises; 3 Combinational Logic Design; 3.1 Introduction; 3.2 Minimization of Boolean Expressions; 3.3 Karnaugh Maps; 3.3.1 Don't Care Conditions; 3.3.2 The Complementary Approach; 3.4 Quine-MCCLuskey Method; 3.4.1 Simplification of Boolean Function with Don't Cares; 3.5 Cubical Representation of Boolean Functions; 3.5.1 Tautology; 3.5.2 Complementation Using Shannon's Expansion; 3.6 Heuristic Minimization of Logic Circuits; 3.6.1 Expand; 3.6.2 Reduce; 3.6.3 Irredundant  
 3.6.4 Espresso 3.7 Minimization of Multiple-Output Functions; 3.8 NAND-NAND and NOR-NOR Logic; 3.8.1 NAND-NAND Logic; 3.8.2 NOR-NOR Logic; 3.9 Multilevel Logic Design; 3.9.1 Algebraic and Boolean Division; 3.9.2 Kernels; 3.10 Minimization of Multilevel Circuits Using Don't Cares; 3.10.1 Satisfiability Don't Cares; 3.10.2 Observability Don't Cares; 3.11 Combinational Logic Implementation Using EX-OR and AND Gates; 3.12 Logic Circuit Design Using Multiplexers and Decoders; 3.12.1 Multiplexers; 3.12.2 Demultiplexers and Decoders; 3.13 Arithmetic Circuits; 3.13.1 Half-Adders; 3.13.2 Full Adders  
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 4.5 Timing in Synchronous Sequential Circuits 4.6 State Tables and State Diagrams; 4.7 Mealy and Moore Models; 4.8 Analysis of Synchronous Sequential Circuits; Exercises; References; 5 VHDL in Digital Design; 5.1 Introduction; 5.2 Entity and Architecture; 5.2.1 Entity; 5.2.2 Architecture; 5.3 Lexical Elements in VHDL; 5.4 Data Types; 5.5 Operators; 5.6 Concurrent and Sequential Statements; 5.7 Architecture Description; 5.8 Structural Description; 5.9 Behavioral Description; 5.10 RTL Description; Exercises; 6 Combinational Logic Design Using VHDL; 6.1 Introduction  
 6.2 Concurrent Assignment Statements

## Sommario/riassunto

A major objective of this book is to fill the gap between traditional logic design principles and logic design/optimization techniques used in practice. Over the last two decades several techniques for computer-aided design and optimization of logic circuits have been developed. However, underlying theories of these techniques are inadequately covered or not covered at all in undergraduate text books. This book covers not only the "classical" material found in current text books but also selected materials that modern logic designers need to be familiar with.